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09/536,452	03/28/2000	Ronny Ronen	02207/8754	5160

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WASHINGTON, DC 20005

EXAMINER

HUISMAN, DAVID J

ART UNIT	PAPER NUMBER
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2183

DATE MAILED: 11/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/536,452

Applicant(s)

RONEN ET AL.

Examiner

David J. Huisman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-15 and 17-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,4-15 and 17-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 11 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. Claims 1-2, 4-15, and 17-23 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 10/4/2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-15, and 17-23 is rejected under 35 U.S.C. 102(b) as being anticipated by Killian et al., U.S. Patent No. 5,420,992 (as applied in the previous Office Action and herein referred to as Killian).

5. Referring to claim 1, Killian has taught a processor comprising:

a) means for executing an instruction of an application of a first bit size ported to a second bit size environment, the second bit size being greater than the first bit size. See column 2, lines 7-33.

b) means for confining the application to a first bit size address space subset (see column 19, lines 36-40), said means for confining comprising:

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(i) means for truncating generated address references of the second bit size to the first bit size. See Fig. 5D and note that the 64-bit virtual address is truncated by removing the upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.

(ii) means for extending to the second bit size the truncated generated address references based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address references and a second setting of the address format control signal to indicate sign-extension of the truncated generated address references. Looking at Fig. 5D, it should be realized that the virtual address is in sign-extended form (column 17, lines 15-24). The upper 32 bits of the address (sign extension bits) are then separated from the rest of the address and fed into the multiplexer 172, thereby truncating the virtual address. As seen from Fig. 5D, the multiplexer would then have two 32-bit inputs; the first being 32 zeroes and the second being the 32 sign-extension bits. One of the inputs will be selected by the multiplexer, resulting in either zero-extending (if the 32 zeroes are selected) or sign-extending (if the 32 sign bits are selected) the truncated virtual address. A single signal, i.e., the "32-bit user mode" signal, is used to determine the output of the multiplexer. That is, this signal (i.e., address format control signal) will select either zero-extension or sign-extension of the address.

6. Referring to claim 2, Killian has taught a processor as described in claim 1. Killian has further taught that the first bit size is 32-bit and the second bit size is 64-bit. See column 3, lines 30-31, and column 5, lines 8-19.

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7. Referring to claim 4, Killian has taught a processor as described in claim 1. Killian has further taught that the means for confining includes means for generating an address fault. See column 11, lines 3-5. The 32-bit address (which would be represented as an extended 64-bit number in the 64-bit environment) that is used to select a memory location in the address space subset is checked for a certain value and if that value exists, then an address error exception will occur.

8. Referring to claim 5, Killian has taught a processor as described in claim 1. Killian has further taught that the means for extending includes means for determining that the first bit size address space subset is signed address space. See column 19, lines 36-40. From this passage it can be seen that the address space is from -2^{31} to $(2^{31}-1)$ which is also known as -2GB to +2GB.

9. Referring to claim 6, Killian has taught a processor as described in claim 1. Killian has further taught that the means for extending includes means for determining that the first bit size address space subset is unsigned address space. See column 13, lines 10-27, and Table 3A. Killian has disclosed Load-Byte-Unsigned (LBU) and Load-Halfword-Unsigned (LHU) instructions, which are zero-extended as opposed to sign extended. As an example, LBU will retrieve an 8-bit value from memory/cache, and zero-extend it to 64-bits, regardless of the most significant bit position. If this unsigned data were then used as an address to access memory, which is possible since Killian has also disclosed indirect jumps in Table 5B (where the contents of a specified register are used as an address to access memory), it would follow that the address space would be unsigned.

10. Referring to claim 7, Killian has taught a processor comprising:

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- a) a memory to store an instruction of an application ported from a first bit size environment to a second bit size environment, the second bit size being greater than the first bit size. See Fig. 1 and column 7, lines 49-54. Note the existence of main memory and an instruction cache.
- b) an instruction execution core coupled to said memory, said instruction execution core to execute the instruction of the application. See Fig. 1. Note that data and instructions are retrieved from memory/cache by the EIC (component 25) and propagated along bus 30 to the execution unit.
- c) said instruction execution core to determine that the application is confined to a first bit size address space subset. See column 19, lines 36-40.
- d) said instruction execution core to generate an address reference of the second bit size as part of execution of the instruction. See column 12, lines 26-65. Also, see Fig. 5D and note that a virtual address is generated (at the middle of the page).
- e) said instruction execution core to truncate the generated address reference from the second bit size to the first bit size. See Fig. 5D and note that the 64-bit virtual address is truncated by removing the upper 32 bits of the address (VA(63..32)), which are then sent to a multiplexer 172.
- f) said instruction execution core to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on a setting of an address format control signal, a first setting of the address format control signal to indicate zero-extension of the truncated generated address reference and a second setting of the address format control signal to indicate sign-extension of the truncated generated address reference. Looking at Fig. 5D, it should be realized that the virtual address is in sign-extended form (column 17, lines 15-24). The upper 32 bits of the address (sign extension bits) are then separated from the rest of the

address and fed into the multiplexer 172, thereby truncating the virtual address. As seen from Fig.5D, the multiplexer would then have two 32-bit inputs; the first being 32 zeroes and the second being the 32 sign-extension bits. One of the inputs will be selected by the multiplexer, resulting in either zero-extending (if the 32 zeroes are selected) or sign-extending (if the 32 sign bits are selected) the truncated virtual address. A single signal, i.e., the “32-bit user mode” signal, is used to determine the output of the multiplexer. That is, this signal (i.e., address format control signal) will select either zero-extension or sign-extension of the address.

11. Referring to claim 8, Killian has taught a processor as described in claim 7. Killian has further taught that the application ported from a first bit size environment to a second bit size environment is an application ported from a 32-bit environment to a 64-bit environment. See column 3, lines 30-31, and column 5, lines 8-19.

12. Referring to claim 9, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to determine that the application is confined to a first bit size address space subset based at least in part on an address space control flag. See column 17, lines 25-27. Note from columns 17-19, that based on the different modes, different address space subsets are used.

13. Referring to claim 10, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to extend the truncated, generated address reference from the first bit size to the second bit size based at least in part on an address format control flag. Recall from the very top of Fig.5E of Killian that a “32-bit user mode” signal exists. This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended. Furthermore, this signal will be

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stored as a flag in a status register, which is described in column 17, lines 25-31. This register comprises flags which specify parameters of the system including the bit-mode (32 or 64) in which the system operates and the type of mode (user, supervisor, kernel) in which it operates. Therefore, the “32-bit user mode” flag will originate in the status register.

14. Referring to claim 11, Killian has taught a processor as described in claim 7. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on a comparison of the generated address reference and the extended, truncated, generated address reference. Recall from previous rejections that a generated 32-bit number is extended to a 64-bit number in Killian’s system. From column 17, line 61, to column 18, line 7, Killian has disclosed that bit 31 of the 64-bit number is checked. If that value is 0, then an address fault has not occurred. However, if that value is 1, then an address exception has occurred. Bit 31, in a sense, represents an overflow bit in that when that bit is set, then the 32-bit application has crossed the 32-bit address space boundary and a fault has occurred. It should be noted that a comparison would inherently be performed to check bit 31. And, this comparison is related to both the original 32-bit address and the extended 64-bit version.

15. Referring to claim 12, Killian has taught a processor as described in claim 11. Killian has further taught that the instruction execution core is to generate an address fault flag based at least in part on an address fault control flag. See Fig.5E. In the upper-right corner of the figure, different types of address faults (R3ERR, R2ERR, R1ERR, and R0ERR) are coupled to a multiplexer which is controlled by an address fault control flag VA(63..62). This value is used to help generate an address fault flag (output line denoted as ADDRESS ERROR), if one exists for the corresponding mode.

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16. Referring to claim 13, Killian has taught a processor as described in claim 7. Killian has further taught that the memory is a cache memory. See column 7, lines 50-52.

17. Referring to claim 14, Killian has taught a processor as described in claim 7. Killian has further taught that the processor is a 64-bit processor. See column 2, lines 16-41, and column 3, lines 30-31. Killian has disclosed that the registers and data path, along with memory addresses, are 64 bits wide. Therefore, Killian has taught a 64-bit processor.

18. Referring to claim 15, Killian has taught a method to confine an application to an address space subset, the method comprising the steps performed by the processor of claim 7. Therefore, claim 15 is rejected for the same reasons set forth in the rejection of claim 7.

19. Referring to claim 17, Killian has taught a method as described in claim 16.

Furthermore, claim 17 is rejected for the same reasons set forth in the rejection of claim 8.

20. Referring to claim 18, Killian has taught a method as described in claim 15.

Furthermore, claim 18 is rejected for the same reasons set forth in the rejection of claim 9.

21. Referring to claim 19, Killian has taught a method as described in claim 15.

Furthermore, claim 19 is rejected for the same reasons set forth in the rejection of claim 10.

22. Referring to claim 20, Killian has taught a method as described in claim 15. Killian has further taught that extending the truncated, generated address reference from the first bit size to the second bit size includes sign-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on the address format control flag. Recall from the very top of Fig. 5E of Killian that a "32-bit user mode" signal exists. This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended. See column 3, line 67, to column 4, line 10. Furthermore,

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this signal will be stored as a flag in a status register, which is described in column 17, lines 25-

31. This register comprises flags which specify parameters of the system including the bit-mode (32 or 64) in which the system operates and the type of mode (user, supervisor, kernel) in which it operates. Therefore, the “32-bit user mode” flag will originate in the status register.

23. Referring to claim 21, Killian has taught a method as described in claim 15. Killian has further taught that extending the truncated, generated address reference from the first bit size to the second bit size includes zero-extending the truncated, generated address reference from the first bit size to the second bit size based at least in part on the address format control flag. Recall from the very top of Fig. 5E of Killian that a “32-bit user mode” signal exists. This signal, when set, would indicate that addresses should be zero-extended and when cleared would indicate that addresses should be sign-extended. See column 3, line 67, to column 4, line 10. Furthermore, this signal will be stored as a flag in a status register, which is described in column 17, lines 25-31. This register comprises flags which specify parameters of the system including the bit-mode (32 or 64) in which the system operates and the type of mode (user, supervisor, kernel) in which it operates. Therefore, the “32-bit user mode” flag will originate in the status register.

24. Referring to claim 22, Killian has taught a method as described in claim 15. Furthermore, the processor of claim 11 performs the method of claim 22. Therefore, claim 22 is rejected for the same reasons set forth in the rejection of claim 11.

25. Referring to claim 23, Killian has taught a method as described in claim 22. Furthermore, the processor of claim 12 performs the method of claim 23. Therefore, claim 23 is rejected for the same reasons set forth in the rejection of claim 12.

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Response to Arguments

26. Applicant's arguments filed on October 4, 2004, have been fully considered but they are not persuasive.

27. Applicant argues the novelty/rejection of claim 1 on page 8 of the remarks, in substance that:

"...applicants respectfully submit that Killian et al. does not anticipate at least the address format aspect of the invention recited in the independent claims, as the virtual address space in Killian et al. is all signed. In Killian et al., whether to choose zero-extension or sign extension for the address space is a question depending upon timing constraints considered when designing the address translation unit, not on the format of a particular address."

28. These arguments are not found persuasive for the following reasons:

a) Applicant appears to be arguing limitations which do not appear in the claims. That is, there is no language in the current claims which connects the address control flag to the type of address space used. The claim merely states that an address format control flag indicates zero or sign extension, and Killian's flag provides such indications. This flag specifies the format of the address, i.e., whether it will be extended with all 0's or extended with the sign bit. In addition, applicant has used the word "comprising" which leaves the claim "open". More specifically, when using "comprising," the prior art may have additional elements which are not recited in applicant's claims and still anticipate the claims. In this situation, applicant has not excluded timing constraints as being a factor in choosing zero or sign extension. Therefore, Killian may still implement these timing constraints and anticipate applicant's claims because Killian has still taught each of the limitations set forth in claim 1, for instance.

29. Applicant argues the novelty/rejection of claim 11 on page 8 of the remarks, in substance that:

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"Additionally, dependent claim 11 recites generation of an address fault flag based at least in part on a comparison of the generated address reference (of the second bit size; see claim 7) and the extended, truncated, generated address reference (also of the second bit size; see claim 7). This feature is not disclosed in Killian et al. Killian et al. discloses a check of twos-complement overflow, as alluded to by the examiner in paragraph 14 of the Office Action. However, this check is performed before the address is sign-extended, as the results are used to decide whether address sign-extension will even be performed. See, e.g., Killian et al. col. 3, lines 64-66. No comparison is made between the N-bit address before sign extension and after truncation/sign extension. Similar features are recited in claims 4 and 22. Reconsideration is requested."

30. These arguments are not found persuasive for the following reasons:

a) Applicant argues that extension is performed in response to a check for two's complement overflow. However, the examiner believes that all Killian is saying is that in 32-bit user-mode, sign-extension (in this case 0-extension) must always occur for a 32-bit address, even when two's complement overflow does occur. The examiner would like to direct applicant's attention to Fig. 5D. Note the generated 64-bit virtual address in the middle of the page represented by the box labeled "virtual address". As the address continues through the system, it is first truncated, sending the upper 32 bits to mux 172. The next highest twenty bits (31:12) are then recombined with the "extension" bits outputted by mux 172 (in 32-bit user mode, the extension bits selected are all 0's). Note that the recombination (extension) occurs before the address (or a portion of the address) is sent to the "address test and control" component. This is clear because the 32 extension bits are combined with 20 other address bits (forming a 52-bit address portion). The address test and control component is the component which checks for an address fault. See Fig. 5E and note that the logic shown makes up the address test and control component. Most specifically, at the very top, it should be realized that R0ERR is produced if the 31st bit of the address is a 1. Therefore, it can be seen that the address is first extended and then the fault is determined (i.e., a bit comparison of the generated address and the extended truncated address occurs. It is a comparison of both addresses because both addresses may be the exact same

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address. Note that the claim does not say that the address are compared to one another...just that a comparison occurs). In the previous (and above rejection), the examiner is not trying to say that the fault is based on two's complement overflow but instead that the 31st bit is an overflow bit in the sense that if it is set, the address has crossed it's valid address space boundary, which is a fault.

Conclusion

31. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

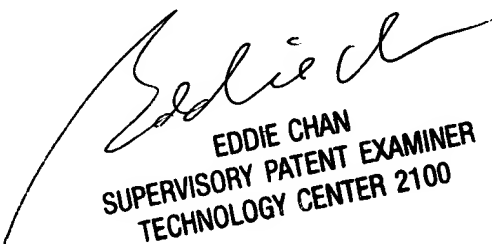
Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (571) 272-4168. The examiner can normally be reached on Monday-Friday (8:00-4:30).

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJH
David J. Huisman
November 15, 2004



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